ADAC Japan
2017

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FUJITSU

shaping tomorrow with you

Fujitsu processor history and future

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Agenda

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- **K computer**
- **Fujitsu processor development history**
  - HPC
  - UNIX/Mainframe
- **Future development plan**
  - Post K
  - AI processor: DLU
- **Summary**

RIKEN K computer

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WR#1

10.51 PFlops (2011/11)


TOP500 CERTIFICATE

K computer, a Fujitsu System at the RIKEN Advanced Institute for Computational Science (AICS), Kobe, Japan

is ranked

No. 1

among the World's TOP500 Supercomputers
with 10.51 PFlop/s Linpack Performance
on the TOP500 List published at the SC11 Conference, November 15, 2011

Congratulations from the TOP500 Editors

Hans Meuer, University of Mannheim
Erich Strohmaier, NERSC/Berkeley Lab
Jack Dongarra, University of Tennessee
Horst Simon, NERSC/Berkeley Lab

K computer “Still the best”

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	2011	2012	2013	2014	2015	2016
1.TOP500 List		2	4	4	4	7
2. Gordon Bell Prize						Finalist
3. HPC Challenge Awards (HPC、Random Access、STREAM、FFT)						
4. Graph500			4	 2		

K computer "High reliable"

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CPU failure rates of the K computer are about quarter compared to that of Blue Waters.

RIKEN Advanced Institute for Computational Science

Monthly Failure Rate of CPUs

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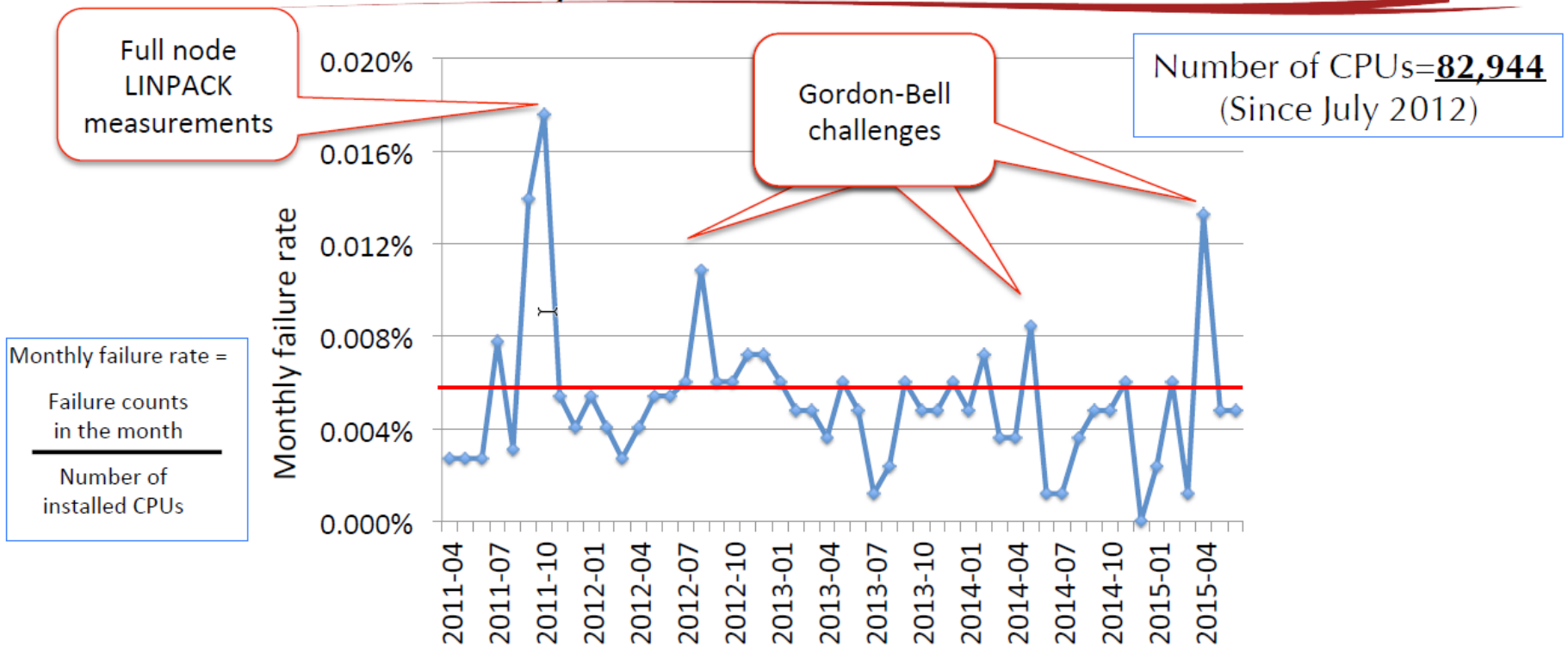

Failure trend of CPUs is almost stable except high load terms

8

HPC in Asia@Frankfurt, Germany 2015

K computer

(Source: ISC 2015 Long term failure analysis of 10 petascale supercomputer, RIKEN)

Fujitsu technologies to realize K computer

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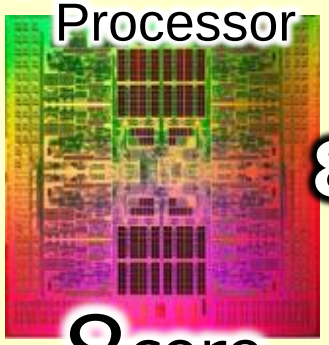
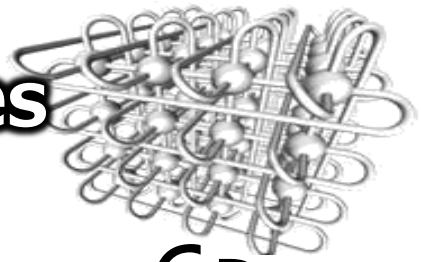
High Performance Processor



8core

864 racks
82,944 Compute nodes
5,184 IO nodes

Torus network



6D.

Liquid Cooling

4processor

K computer

High density rack

24board

「京」は、理化学研究所が2010年7月から使用している「次世代スーパーコンピュータ」の愛称です。

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Fujitsu processor development History
- HPC
- UNIX/GS

Fujitsu Processor development

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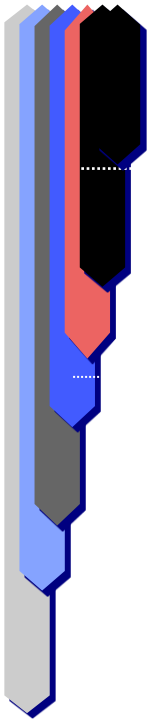
Perpetual evolution, Always targeting No.1



Virtual Machine Architecture
Software on Chip
High-speed Interconnect

HPC-ACE
System on Chip
Hardware Barrier

Multi-core Multi-thread

L2$ on Die

Non-Blocking $
O-O-O Execution
Super-Scalar

Single-chip CPU

Store Ahead
Branch Histor
Prefetch

$ ECC
Register/ALU Parity
Instruction Retry
$ Dynamic Degradation
Error Checkers/History

Performance

Reliability

AI

DLU

Post-K ARM

HPC

UNIX

20nm

SPARC64 XIfx

40nm

SPARC64 IXfx

45nm

SPARC64 VIIIfx

SPARC64 X+

SPARC64 X

SPARC64 XII

Next GS

65nm

SPARC64 VII

GS21 2600

90nm

SPARC64 VI

SPARC64 V+

GS21 1600

130nm

SPARC64 V

GS21 900

28nm

180nm

GS21 600

Mainframe

250nm / 220nm

GS8900

GS8800

GS8800B

SPARC64 GP

350nm

GS8600

SPARC64 GP

SPARC64 II

SPARC64

Technology generation

Mainframe/UNIX/HPC + AI incremental development

2000～2003 2004～2007 2008～2011 2012～2015 2016～

SPARC64™ VII

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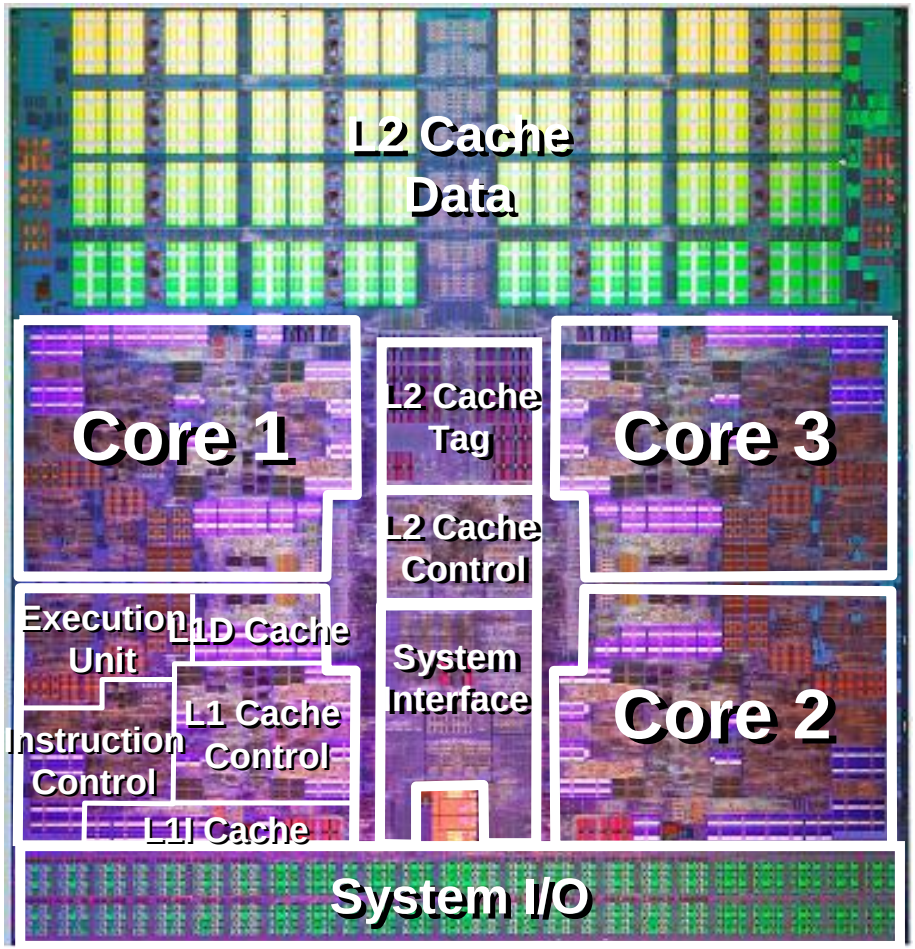

- Architecture Features
  - 4core x 2threads (SMT)
  - Embedded 6MB L2$
  - 2.5GHz
  - Jupiter Bus
- Fujitsu 65nm CMOS
  - 21.31mm x 20.86mm
  - 600M transistors
  - 456 signal pins
- 135 W (max)
  - 44% power reduction per core from SPARC64™ VI

SPARC64™ VII in HPC & UNIX server

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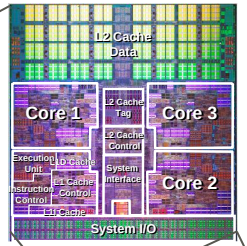
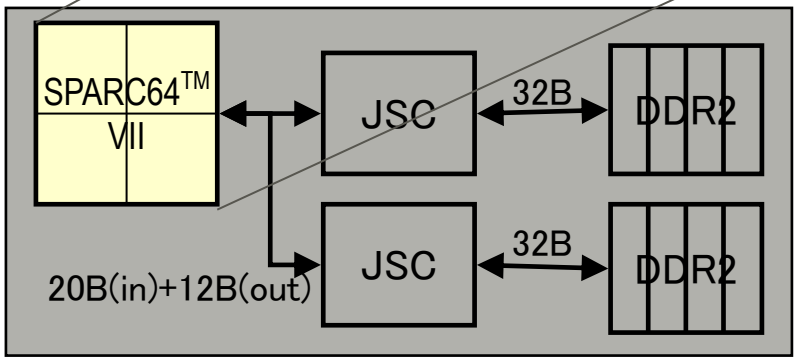
The same processor was used both in HPC and UNIX severs
- SC(system controller LSI) was different

Supercomputer FX1

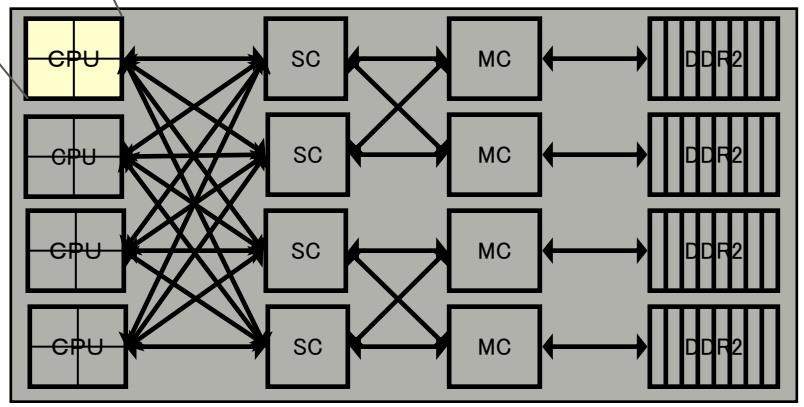


SPARC Enterprise

System board diagram



System board diagram



SPARC64™ VIIIfx Chip [HPC]

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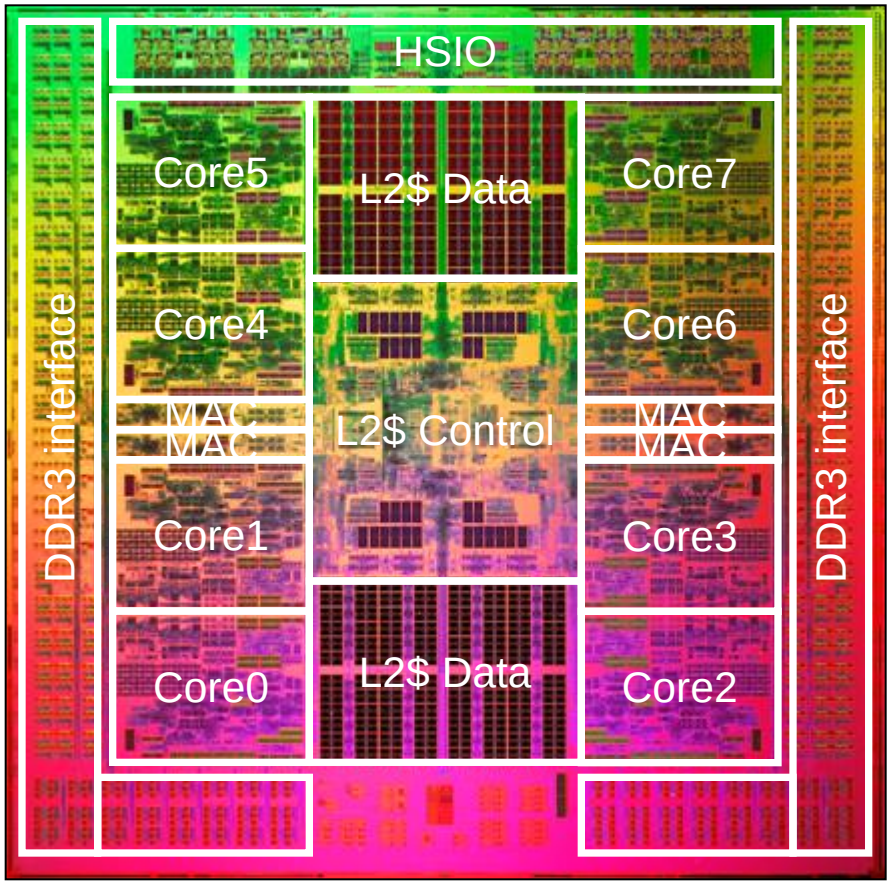

- Architecture Features
  - 8 cores
  - HPC-ACE (128-bit SIMD)
  - Shared 6 MB L2$
  - Embedded Memory Controller
  - 2 GHz
- Fujitsu 45nm CMOS
  - 22.7mm x 22.6mm
  - 760M transistors
  - 1271 signal pins
- Performance (peak)
  - 128GFlops
  - 64GB/s memory throughput
- Power
  - 58W (TYP, 30℃)
  - Water Cooling – Low leakage power and High reliability

SPARC64™ X+ Chip [UNIX]

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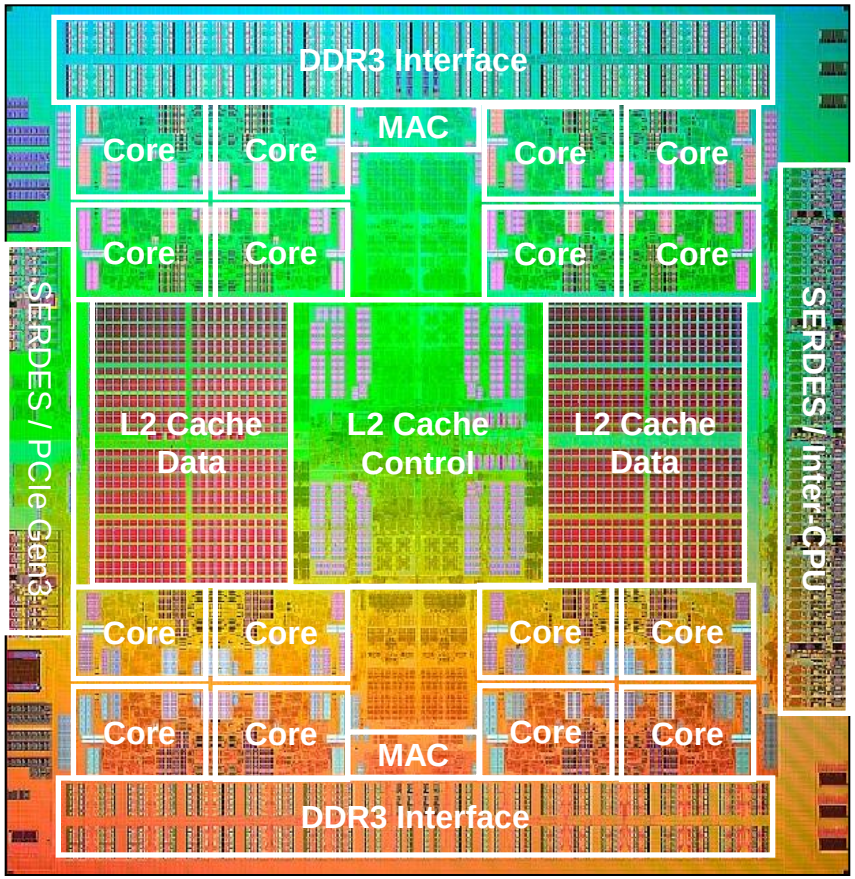

- **Architecture Features**
  - 16 cores x 2 SMT threads
  - Shared 24 MB L2$
  - Memory and I/O Controllers
  - HPC-ACE (128bit SIMD)
  - **SWoC (Software on Chip)**
- **28nm CMOS**
  - 24.0mm x 25.0mm
  - 2,990M transistors
  - 1,500 signal pins
  - 3.7GHz
- **Performance (peak)**
  - 473GFlops
  - 102GB/s memory throughput

SPARC64™ XIfx Chip [HPC]

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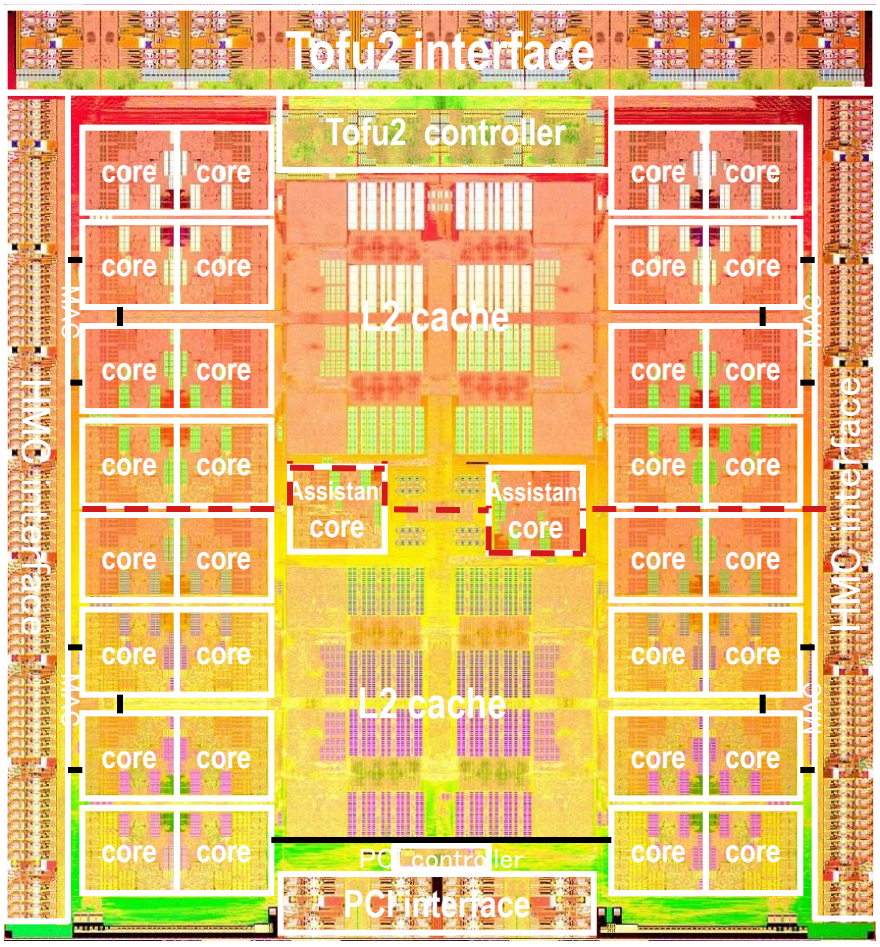
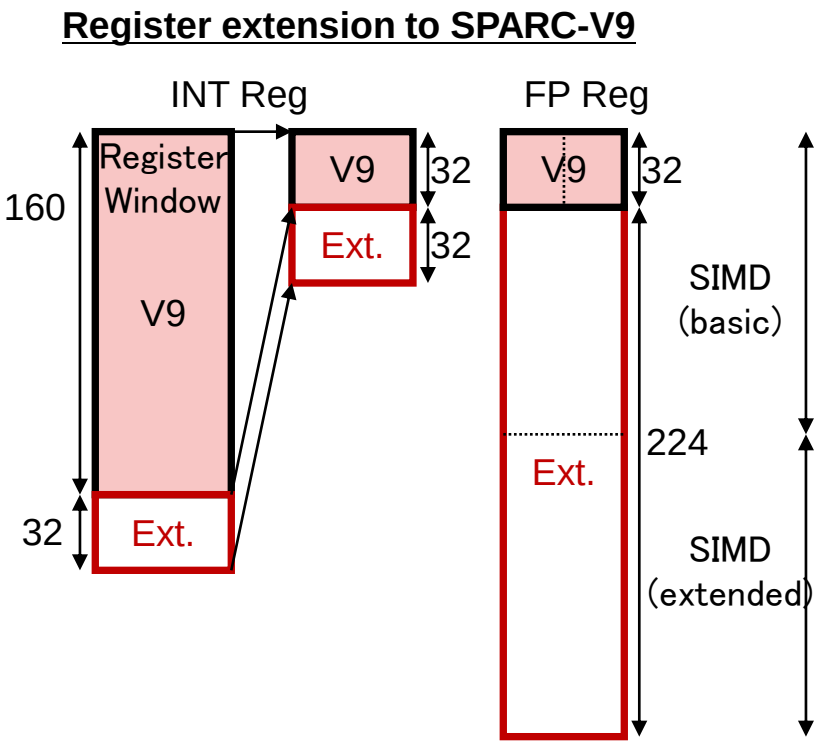


- **Architecture Features**
  - 32 computing cores + 2 assistant cores
  - HPC-ACE2 (256bit SIMD)
  - 24 MB L2 cache
  - HMC, Tofu2 , PCI Gen3
- **20nm CMOS**
  - 3,750M transistors
  - 1,001 signal pins
  - 2.2GHz
- **Performance (peak)**
  - 1.1TFlops
  - HMC 240GB/s x 2(in/out)
  - Tofu2 125GB/s x 2(in/out)

HPC-ACE @SPARC64™ VIIIfx

(High Performance Computing - Arithmetic Computational Extensions)

- Fujitsu's unique ISA extension to SPARC-V9 for HPC
  - Large register sets
  - 128bit SIMD
  - Software controlled Cache
  - FP Trigonometric Functions
  - Conditional operation
  - FP Reciprocal Approximation of Divide/Square-root
- SPARC architecture is tolerant about ISA enhancements.



Software on Chip @SPARC64™ X+

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HW for SW

ISA extensions to accelerates specific software function with HW

The targets

- Decimal operation (IEEE754 decimal and NUMBER)
- Cypher operation (AES/DES)
- Database acceleration

HW implementation

- The HW engines for SWoC are implemented in FPU
  - To fully utilize 128 FP registers & software pipelining
- Implemented as instructions rather than dedicated co-processor to maximize flexibility of SW.
- Avoid complication due to “CISC” type instructions
  - Various “RISC” type instructions are newly defined, instead.
  - 18 insts. for Decimal, and 10 insts. for Cypher operation

SPARC64™ VII Pipeline [HPC/UNIX]

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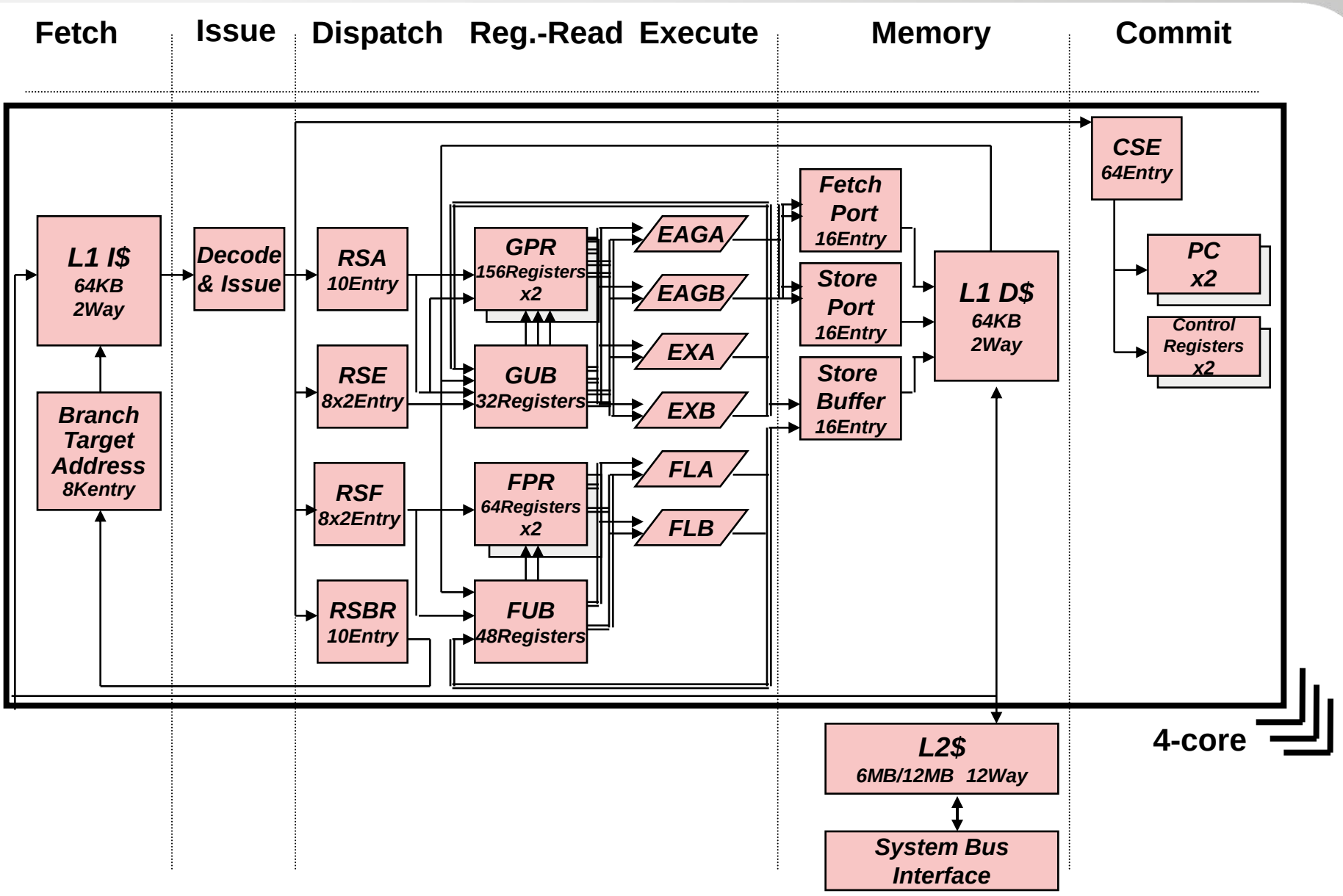

SPARC64™ VIIIfx Pipeline [HPC]

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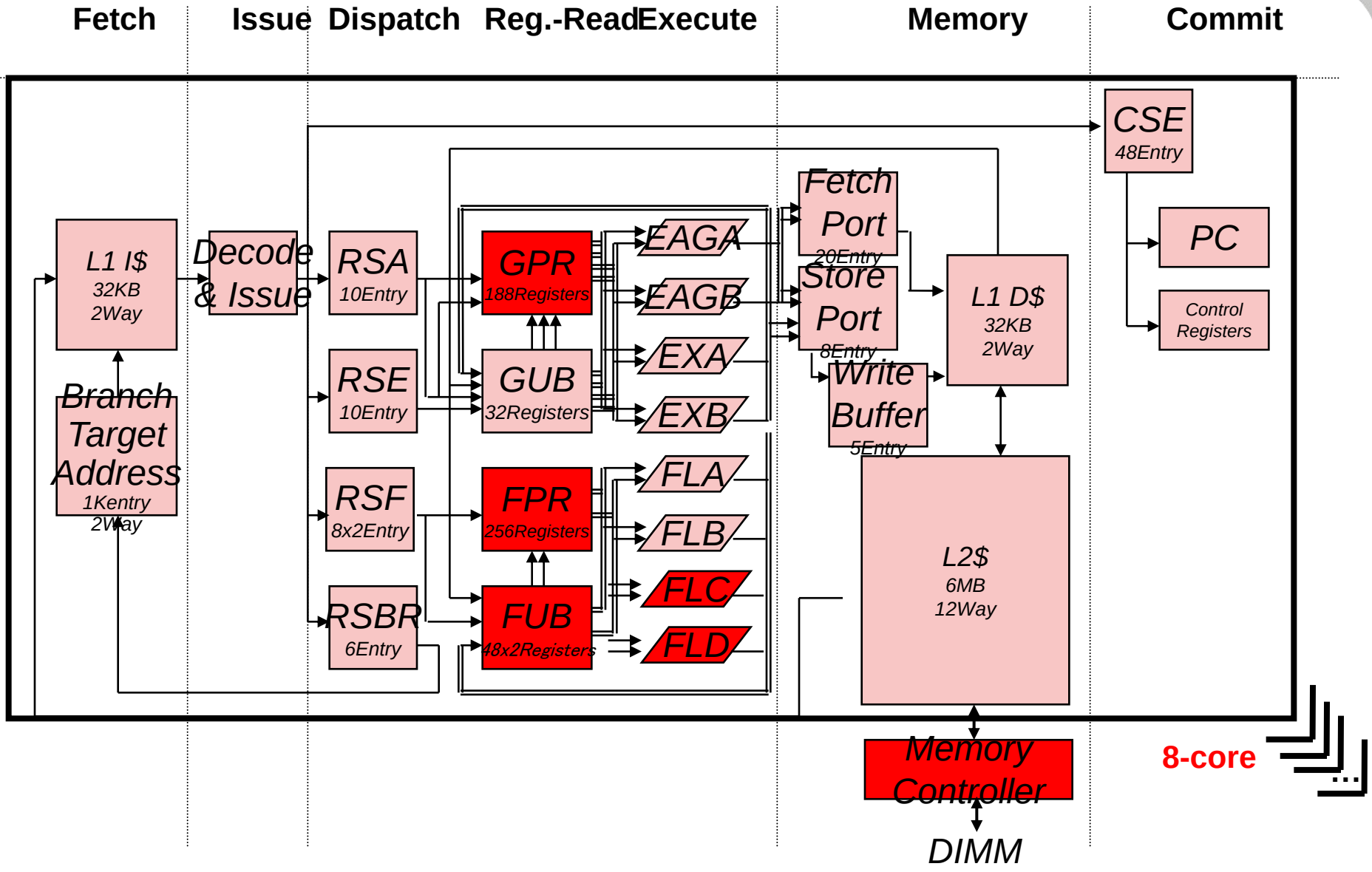

SPARC64™ X Pipeline [UNIX]

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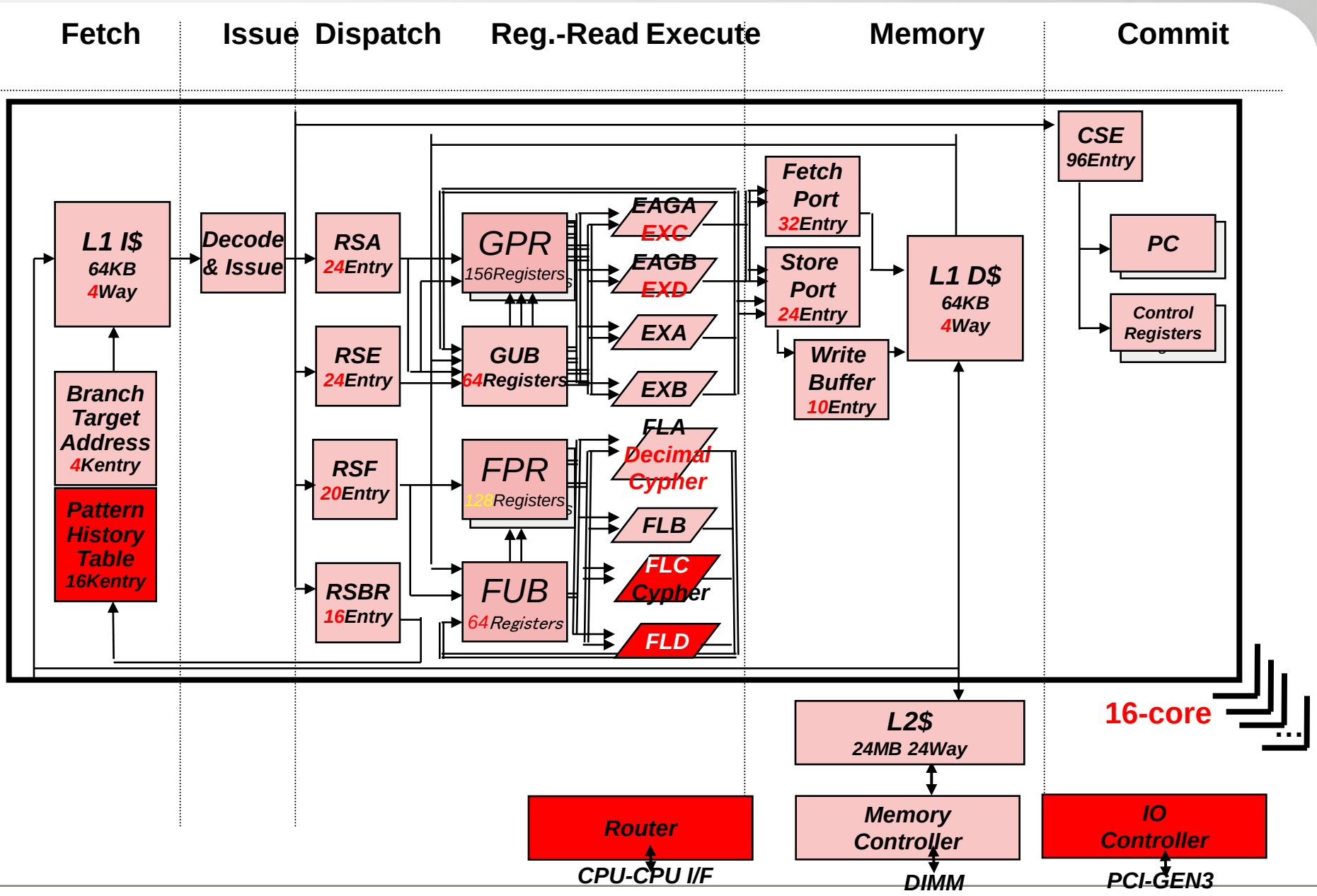

SPARC64™ XIfx Pipeline [HPC]

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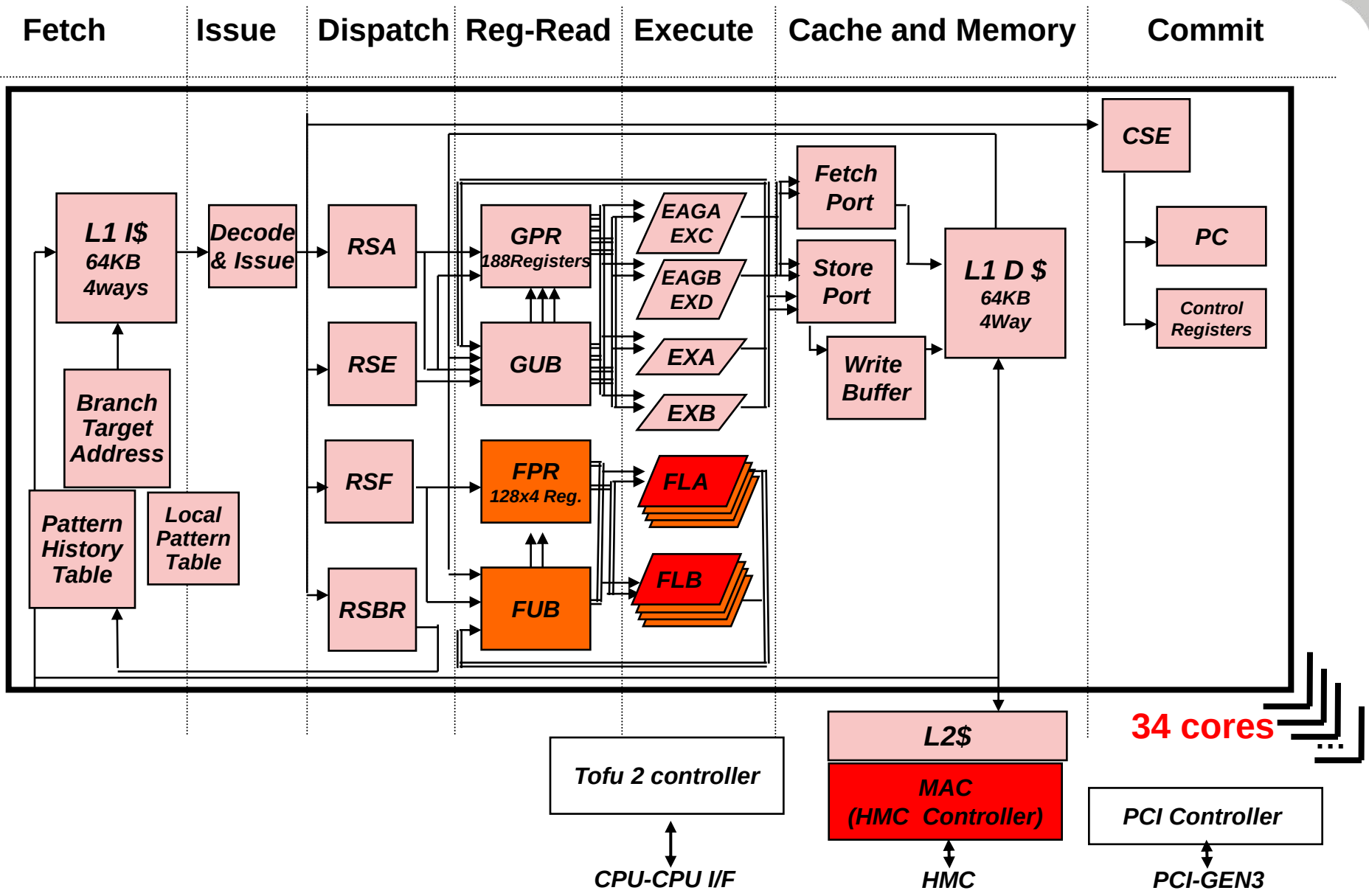
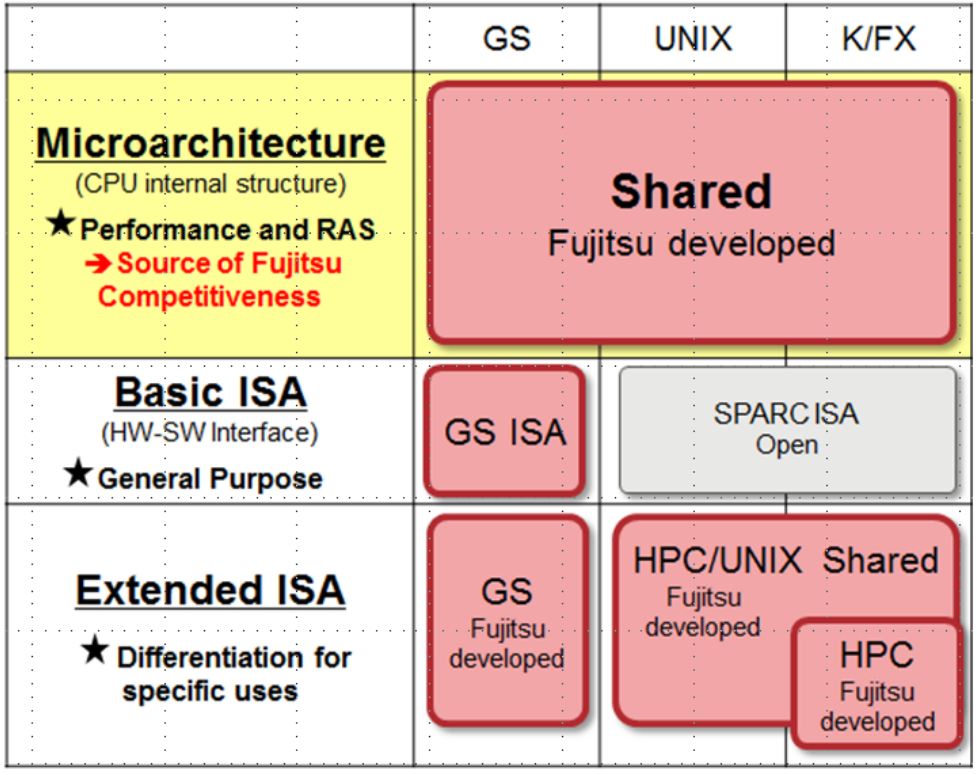
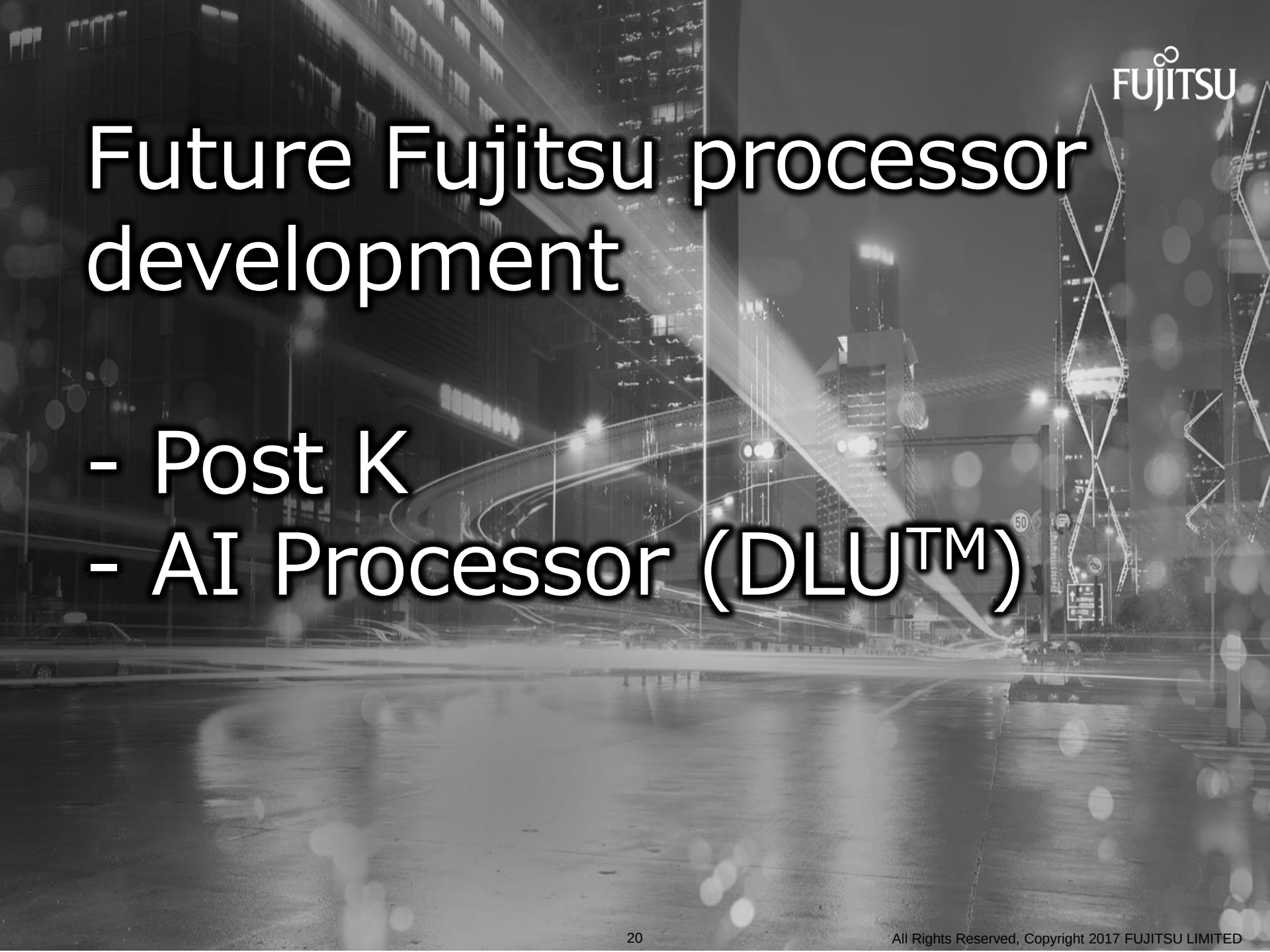


Fujitsu's processor design approach

- **Fully utilize the latest semiconductor technology**
- **Enhance/change ISA (Instruction Set Architecture) to meet requirements:** HPC-ACE, SWoC
- **Shared micro-Architecture across HPC/UNIX/GS**
  - Perpetual evolution over generations





Future Fujitsu processor development

- Post K
- AI Processor (DLU™)

Post-K Goals and Approaches

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Post-K Goals

- High application performance and good power efficiency
- Keeping application compatibility while advancing from predecessors
- Good usability and better accessibility for users

Our Approaches

- Developing high performance and scalable, custom CPU cores
  - 【Performance】 Wider SIMD & high memory BW, mathematical acc. Primitives
  - 【Scalability】 Scalable many core, zero OS jitter (assistant core)
  - 【Power efficiency】 The best device tech, power control functions, optimal resources
- Maintaining performance balance and supporting advanced features
  - High memory BW, “Tofu” interconnect, and RIKEN advanced system software
- Adopting ARM standard architecture
  - Co-operation with ARM/Linux community and utilization of open source software
  - Getting involved in the ARM HPC ecosystem

Post-K CPU

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- **ISA: ARM SVE**
  - FUJITSU, as a lead partner in ARM SVE development, contributes to specification of ARM SVE (Scalable Vector Extension), for application performance
  - FUJITSU ARM core incorporates FUJITSU's proven supercomputer microarchitecture
- ARM SVE, plus optional functions and Tofu, maintain programing models and performance balance
- Post-K complies ARM's standard frameworks (SBSA, etc.), for compatibility among platforms

	Functions for Perf.	Post-K	FX100	FX10	K computer
SVE incorporated	SIMD	512bit	256bit	128bit	128bit
	FMA4	✔	✔	✔	✔
	Math. acc. prim.*	✔Enhanced	✔	✔	✔
Optional functions	Inter-core barrier	✔	✔	✔	✔
	Sector cache	✔Enhanced	✔	✔	✔
	Prefetch modes	✔Enhanced	✔	✔	✔
Interconnect	Tofu	✔Enhanced	✔	✔	✔

*Mathematical acceleration primitives include trigonometric functions, sine & cosines, and exponential...

DLU™ Goals

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K computer

Supercomputer K technologies

FY2018～

DLU™

(Deep Learning Unit)

DLU™ features

- Architecture designed for Deep Learning
- High performance HBM2 memory
- Low power design

➔ Goal: 10x Performance/Watt compared to others

- Massively parallel： Apply the supercomputer interconnect technology

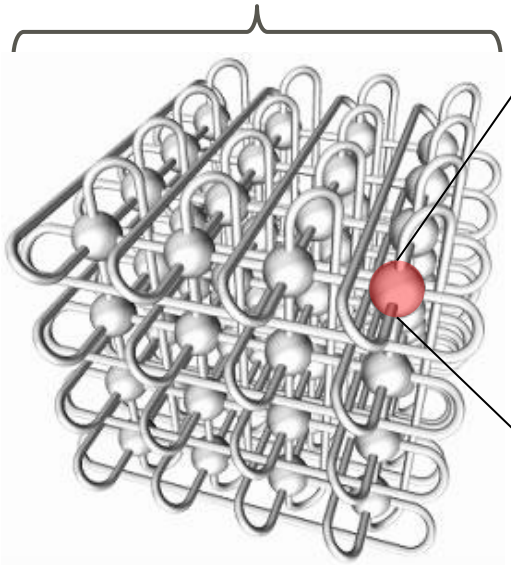
➔Ability to handle large scale neural networks

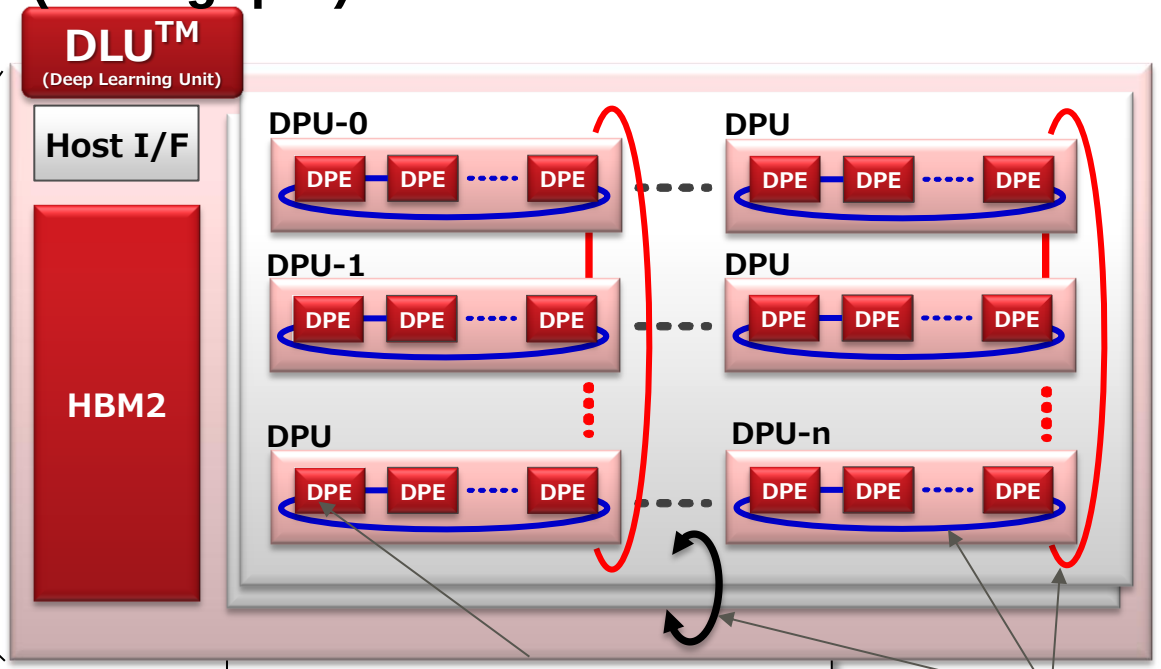
DLU™ architecture

- ISA: Newly developed for Deep learning
- Micro-Architecture
  - Simple pipeline to remove HW complexity
  - On chip network to share data between DPUs
- Utilize Fujitsu's HPC experience such as high density FMA and high speed interconnect

➔ Maximize performance(throughput) / watt

Large scale DLU interconnect through off-chip network





Fujitsu's interconnect technology

New ISA for Deep learning
High density FMA

on-chip network

DPU: Deep learning Processing Unit, DPE: Deep learning Processing Element

DLU™ Future Roadmap

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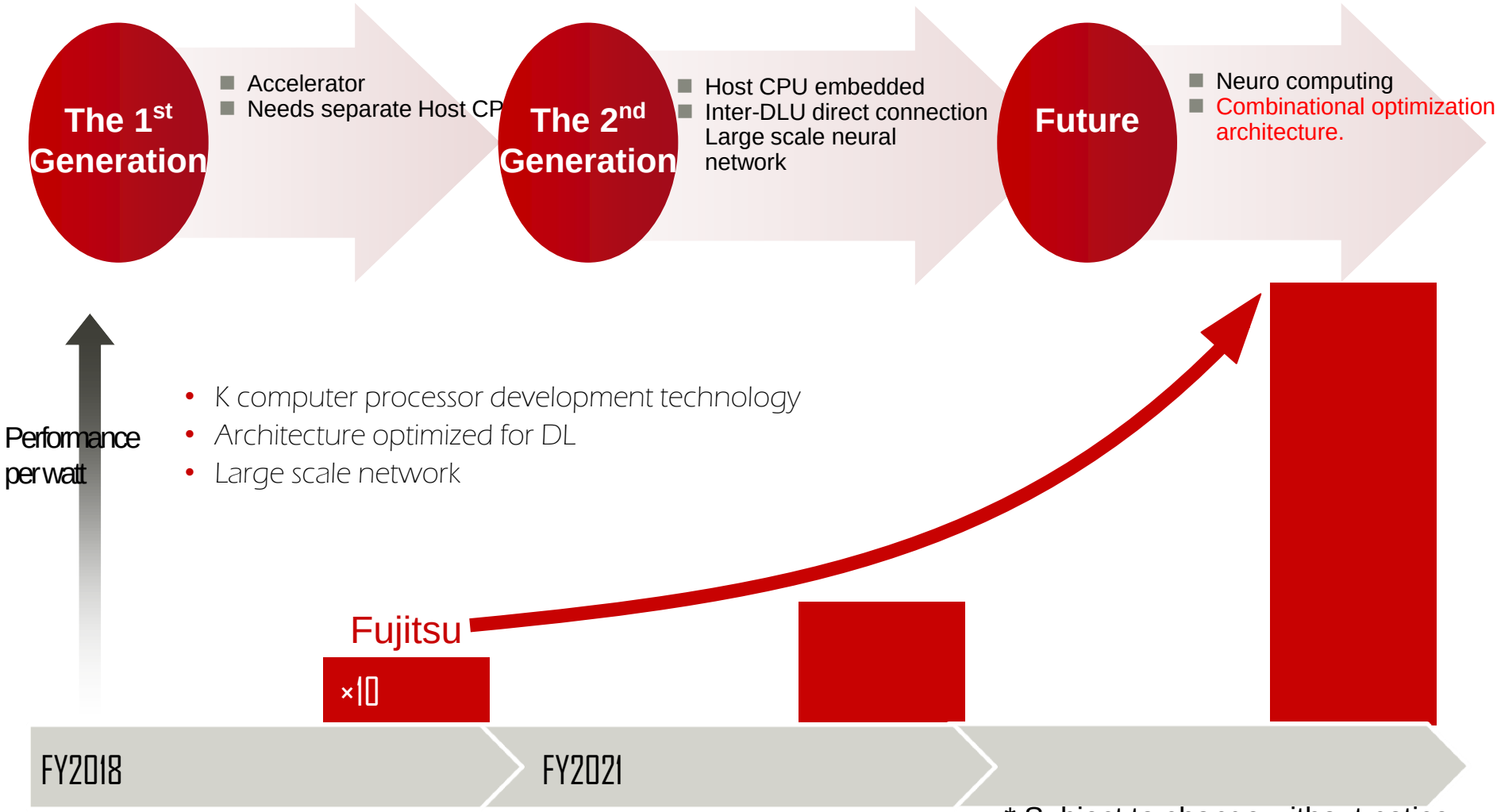
- **Multiple generations of DLUs over time, as we currently do for HPC/UNIX/Mainframe processors.**



* Subject to change without notice

New Arch. Rivals Quantum Computers

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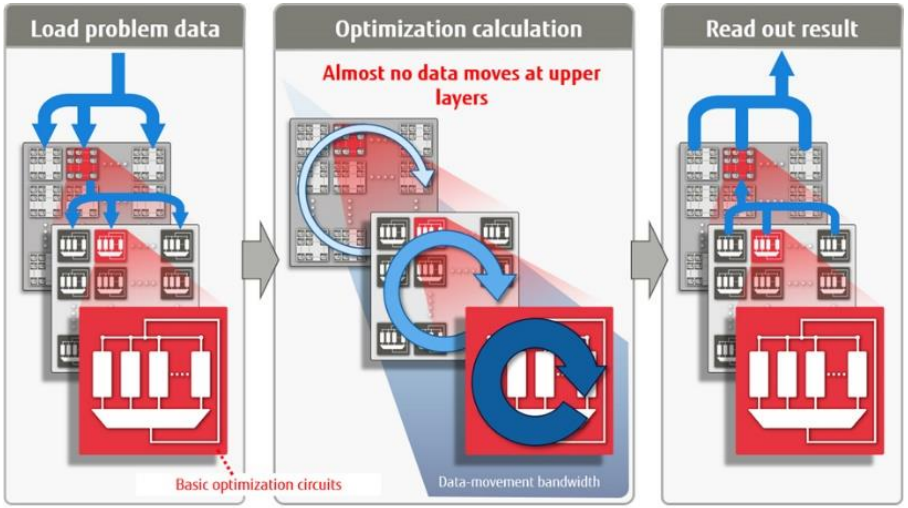
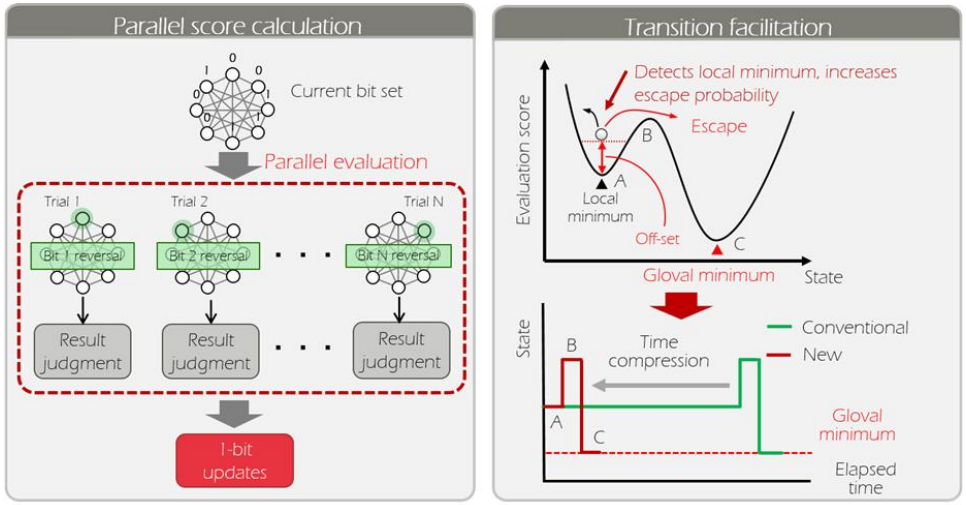
- New Architecture
  - Architecture designed for combinatorial optimization problems
  - Uses a basic optimization circuit, based on digital circuitry and conventional semiconductor technology
  - Hierarchical structure for optimal data movement and parallel calculation
- Acceleration Technology
  - Calculates multiple candidates at once, parallel execution
  - Detects and escapes from the local minimum states by adding score



New architecture



Acceleration using basic optimization circuit

http://www.fujitsu.com/global/about/resources/news/press-releases/2016/1020-02.html

Summary

FJ Processors

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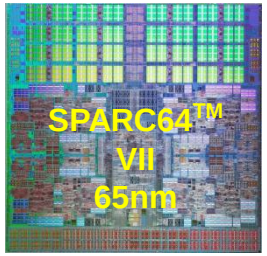
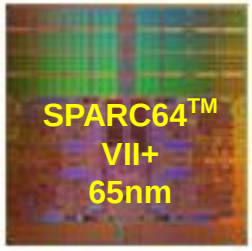
2008
FX1
4core



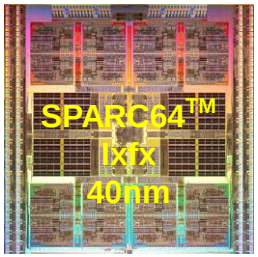
SPARC Enterprise

2010
K Computer
8core

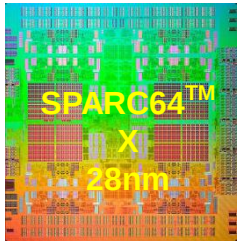
2011
SPARC Enterprise
4core



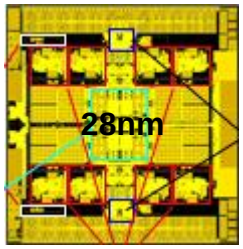
2012
FX10
16core



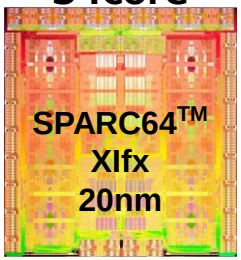
2013
M10
16core



2014
GS21 model 2600
8core



2015
FX100
34core



AI
DLU

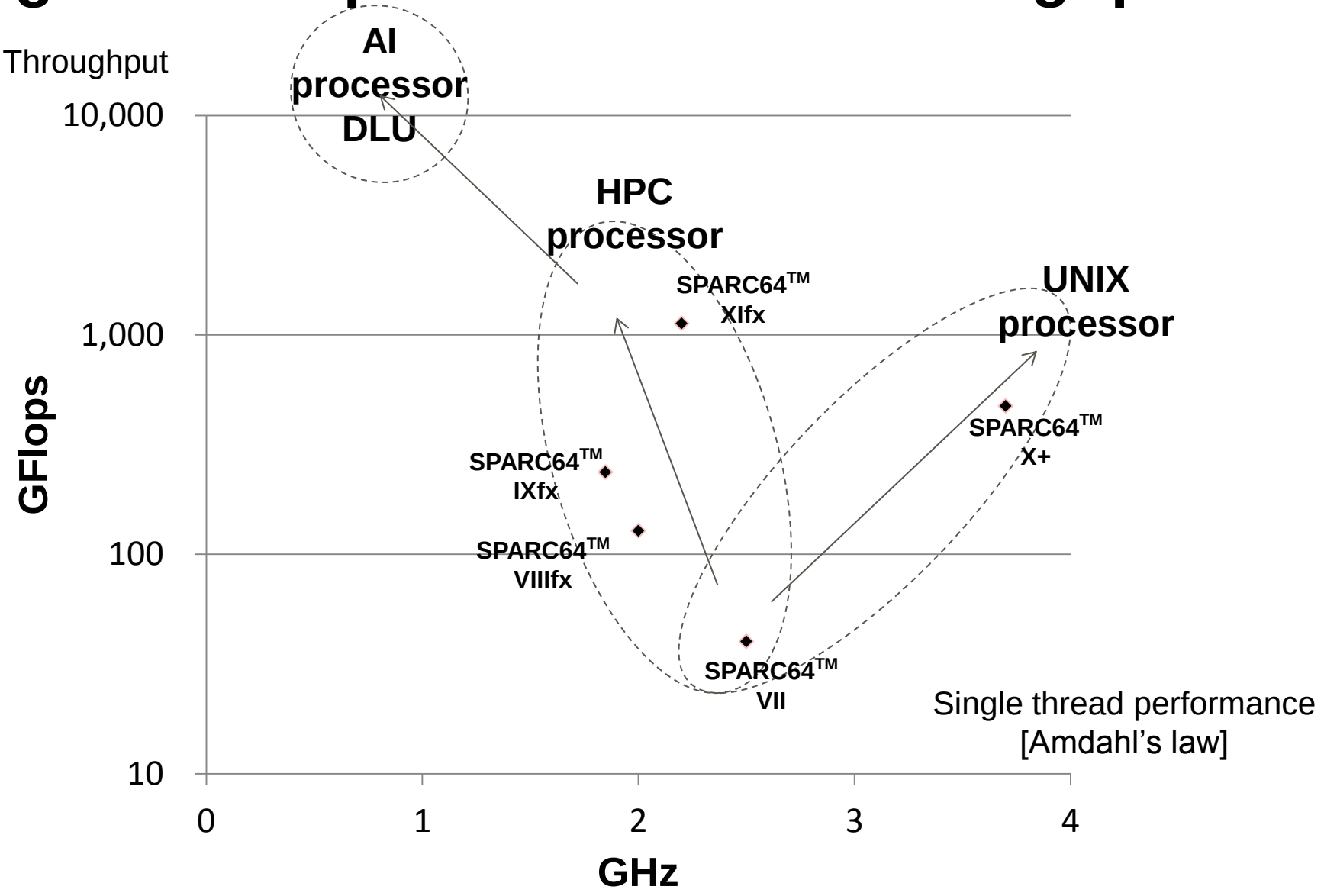
HPC
Post “京”

UNIX
SPARC64™
XII

Mainframe
Next
GS

- Utilization of the latest Semiconductor technologies
- Evolution to meet different requirements between HPC/UNIX/Mainframe/AI

An example of different requirements: Single thread performance vs Throughput



Summary

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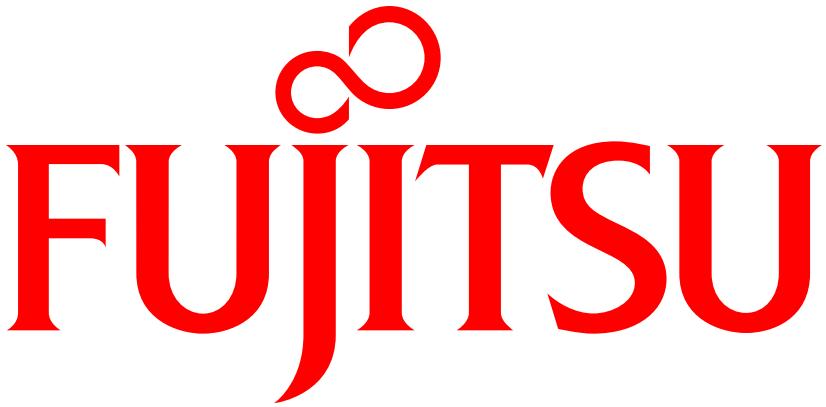
- Fujitsu has successfully designed various processors for decades.
- Fujitsu's processor design win has come from
  - Instruction set architecture (ISA) enhancements
  - Shared micro-architecture with perpetual evolution over generations
  - Semiconductor technology improvements
- Fujitsu will take similar design approach for Post-K and DLU
  - ISA and micro-architecture are getting more important due to the limitation of Moore's law.
- Fujitsu will continue to develop processors to meet the needs of a new era.



shaping tomorrow with you